REMARKS

The Office Action mailed 6/30/04 noted the following:

(1) Informalities in the drawings.

(2) Claims 1-11 were provisionally rejected under obviousness-type double patenting over the claims in applicants copending Application No. 10/413,810 in view of not being patentably distinct.

(3) Claims 1-5 were rejected under Section 102(b) as anticipated by Plus (USPN 4,872,141). Further, claim 6-11 were rejected under Section 103(a) over Plus as being obvious.

(4) Claims 12-16 and 20 were rejected under Section 102(b) or section 103(a) as either anticipated or obvious over Bertin (USPN 6,137,129).

(5) Finally, Claims 17-19 were objected to as being dependent from a rejected base claim, but otherwise allowable.

In response, the drawings and the specification have been amended. Claim 1 is amended to annul the obviousness-type double patenting. Claims 12 and Claim 20 are amended to better present the new subject matter, but are believed to be outside the realm of prior art sited by the examiner. In view of the amendments and arguments presented herewith, the Applicant submits that all claims are in condition for allowance. Withdrawal of the objections is respectfully requested.

Drawings

The corrected drawings per M.P.E.P. § 608.02(g) are enclosed. Withdrawal of the objection is respectfully requested.

Double Patenting

The examiner noted that:

> 4. Claim 1-11 are provisionally rejected under the judicially created doctarine of obviousness-type double patenting as being unpatentable over claims 13-14, 16-18, 1-3, 6-11, and 19 of copending Application No. 10/413,810. Although the conflicting claims are not identical, they are not patentably distinct from each other.
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> This is provisional obviousness-type double patenting rejection because the conflicting claims have not in fact being patented.

Applicant has amended Claim-1 to differentiate the independent claim from those sited in application 10/413,810. The amended Claim-1 specifically draws attention to a method of fabricating latches wherein the high performance inverter (in the latch) is fabricated with logic transistors, in conjunction with logic circuits, on a high performance semiconductor layer. The low performance inverter (in the latch) is separately constructed vertically above the logic transistors to reduce the latch area, and improve the latch performance. The ability to use the substrate layer for logic circuits allow the new latch to be used for Cache memory, CAM, FIFO chains, Flip-flops, single-port RAM, multi-port RAM and many other forms of latch constructions in integrated circuits. These applications are in the embedded memory category. The modified Claim-1 is not limited to high density memory construction, and further not limited to stacking the two inverters one above the other.

In the copending Application 10/413,810, Claims 1-3, 6-11 and 19 pertain to an SRAM cell having a second inverter stacked above a first inverter, without restrictions on how it is constructed. The bottom inverter has a high-mobility conducting path, while the top inverter has a lower mobility conducting path. Those claims do not suggest a method to use logic transistors to construct the first inverter, and to use a second set of thin-film transistors above logic transistors to construct the feed-back inverter for the latch. Claims 13-14, 16-18 in that application refers to a method of making a stacked latch. In that method, fabricating a first inverter in a high-mobility layer is not contingent on fabricating logic transistors to form logic circuits. The copending Application is focused on stand alone high density fast SRAM memory, while the current divisional Application is focusing on embedded memory integrated with logic circuits.

With the amended claims, the applicant respectfully submits that Claim-1 and those depended thereupon no longer fall under obviousness type double patenting. Withdrawal of the objection is respectfully requested.

The Rejections under 35 USC § 102(b)

The examiner noted that:

> 5. Claim 1-5 are rejected under 35 USC 102(b) as being anticipated by Plus et al. U.S. 4,872,141 (the '141 patent).

The applicant has differentiated the new invented matter in the manner in which the two inverters are constructed on vertically separated stacked semiconductor layers. The footprint of the disclosed latch occupies the space of only one inverter, while the other is positioned either above the first inverter or above the logic transistors. This stack feature is not demonstrated in the '141 patent by Plus.

Plus, in Fig-2 shows pyrolitic depositions of layers 52 and 54 side by side on the same substrate layer 50 using two deposition steps. In Fig 3a & 3b, Plus show simultaneous formation of region 52 and 54 in one step. In both embodiments, formation of these layers one above the other is not demonstrated. Plus shows two methods of gate constructions: (i) a common deposition for gate 34 and 34a in m-Si and p-Si respectively, and (ii) two depositions for gates 34 and 34a, wherein p-Si layer 54 is now in common with gate 34 layer. With both of these methods, a stackable transistor construction is not feasible. Furthermore Plus does not demonstrate the value for stacking the two invertors. In Col 2, line 34 Plus states:

> "Further, since the desired output current for inverter 14 is one fifth to one hundredth the desired output current of the inverter 12, and by using p-Si for the inverter 14 and m-Si for inverter 12, the size of cell 10 can be proportionally reduced, while maintaining the same ratio of output impedances of inverters 12 and 14 as in said patent"

Plus attempts to reduce the footprint of the two inverters with p-Si smaller channel length transistors for inverter 14. The ability to move one inverter away would have produced a much more significant savings. The advantage of stacking is summarized by the Applicant in the first paragraph on page 11, line 2 as:

(i) A latch comprises two back to back inverters formed on two separate semiconductor layers.
(ii) A high performance inverter is constructed on a high mobility semiconductor layer.
(iii) A lower performance inverter is constructed in a lower mobility semiconductor layer.
(iv) The two inverters are stacked one above the other to reduce the latch area, and connected back-to-back to provide the necessary feed-back.
(v) This arrangement allows fast access times at a reduced foot-print for high density memory.

Based on Plus patent, one with ordinary skill would not be able to anticipate the novel results as disclosed in Applicant's Claim 1. Withdrawal of the rejection of Claim 1 and those dependent thereupon is requested.

The Rejections under 35 USC § 103(a)

The examiner noted that:

> 6. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (typo?) the '141 patent for being obvious.

The applicant assumes that the examiner refers to Plus (not Miller) with the '141 patent. The Applicant respectfully traverses the rejection for Claims 6-11 which are dependent claims derived from Claim 1. As the base Claim 1 is not anticipated by the '141 patent, withdrawal of the rejection on derivative Claims 6-11 is respectfully requested.

With regards to Claim-10, in addition to being a derivative claim, it also shows a stacked pass-gate constructed in the same semiconductor layer as the stacked inverter. It would not be able to construct a stacked pass-gate transistor using Plus teachings. With respect to Claim-11, Plus does not show a single geometry construction for his inverters: neither inverter 12 nor inverter 14 in Fig-1. To construct a single geometry inverter, the N+ drain of NMOS and P+ drain of PMOS must merge. Plus shows contacts for drain 28a and 28 in Fig-2f indicating these are different geometries. Comparing Fig-1 and Fig-2f, nodes 32 and 32a are seen connected to a common ground supply via metal line 21. However, nodes 28 and 22 are connected together, while nodes 22a and 28a are also connected together. If transistor 16 and 30 are located in a single geometry, it would not require a contact at 28 and a metal strap 72 as shown in Fig-2f.

The Rejections under 35 USC § 102(b) or 103(a)

The examiner noted that:

> 7. Claims 12-16 and 20 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bertin et al. U.S. Patent 6,137,129 (the '129 patent).

Bertin pertains to an SRAM fabrication wherein the pass gates are constructed above the latch elements. There are no logic circuits discussed in his disclosure. The Applicants claims pertain to an SRAM fabrication wherein the latch elements (including pass gates) are constructed above logic circuits. Furthermore, Bertin illustrates a stack die bonding and inter-die wiring technique, while the Applicant illustrates a monolithic single die fabrication and wiring technique.

Bertin in the '129 patent discloses construction of epitaxially grown NFET and PFET pillars sharing a common gate oxide to form a stand alone SRAM cell array. Bertin does not disclose construction of decoder circuits required to access each SRAM cell. Key elements of Bertin latch array are discussed first. Bertin in col 2, line 43 alludes to three specific steps in his embodiment:

> "There are three major steps in the preferred embodiment SRAM process. First, preferred embodiment latches are formed in an insulator layer on a semiconductor wafer, preferably SiO2 on silicon. Second, the cell pass gates are formed on a pass gate layer, referred to herein as an Input/Output (I/O) layer. Third, the I/O layer is bonded to and connected to the latch layer."

This method uses two distinctly different substrate silicon wafers. The first wafer is used to construct vertical FETs in the latches. The second wafer is used to construct pass gates to select and de-select individual latches in a latch array. The two wafers are bonded together and die-to-die wired to obtain the required SRAM functionality. Construction of control logic to access data in the SRAM cell is not disclosed.

The latch formation is described starting in col 3, line 26 and shown in Fig-1 thru Fig-12. Four key components of Bertin are summarized below.

1) An SOI type structure is created by an epitaxial process as discussed starting in col 5, line 23. The substrate wafer is striped patterned with 0.4-1.0 um thick nitride (col 5, line 62), and the space in between filed with TEOS oxide. Gaps are formed thru the nitride to the underlying silicon wafer and N+/P-/N+ stacks are grown epitaxially on the substrate to fill the gaps. The stacks have the same height 0.4-1.0 um as the nitride film. It would not be possible for one with ordinary skill to reduce the epitaxy thickness to below 0.4 um (i.e. 4000 Angstroms) height. Three separate doping regions (see Fig-10B) must be contained inside of the epitaxy film, and metal line contacts (228 in Fig-10B) have to be made to this stack: both dictating construction of thicker films. At 4000 Angstroms, the epitaxy film becomes a thick film layer. The silicon substrate is shown in Fig-10B as layer 210 (and Fig-12B marked with P+ and P- symbols). A single crystal substrate is required to grow an epitaxial film.

2) In a similar second striping and epi growth process sequence, a second P+/N-/P+ stack is epitaxially grown adjacent to the first N+/P-/N+ stack. The second stack is separated by a thin gate oxide from the first stack. This allows direct coupling between the two stacks to form an inverter. Thus there is no gate required for the two inverters, the drain of one acts as the gate for

the other. These directly coupled vertical stacks act as NFET and PFET devices of the inverter that forms a single latch. Two inverters have to be cross coupled by wires to form a latch.

3) As described in col 8, line 7, a tungsten strap metal is deposited on the surface and defined into lines to strap numerous latches together. Extra steps are taken to limit these strap wires locally. First TEOS is deposited over strap metal and planarized. Holes are etched into the TEOS layer to re-expose the tops of the vertical stacks (Fig-10B, stacks 212/224 and 212/224). In the exposed holes, some portions of tungsten lines are etched as shown in Fig-11 to limit the wire connections locally. Then the holes are filled with TEOS again and polished. This cap TEOS is the layer 242 in Fig-12B. In addition to cross coupling, ground and power buses are required for each of the inverters.

4) As described in col 8, line 41, power and ground connections are made by opening large areas of TEOS 240 from the top, depositing, patterning and etching a bus metal layer into 236 & 238 regions as shown in Fig-13A. Latch landing pads 246 in Fig-13B are formed over the TEOS regions adjacent to power and ground lines to bond a second wafer. This second wafer contains the pass gates of the SRAM array. The pad construction mandates bonding from the top.

The pass gate layer is formed on a second wafer. This second wafer is shown in Fig-14 with a separate substrate 264 that is used to construct the pass gate transistors. The construction is described starting in col 8, line 65. The substrate 250 is P-/P+ doped, the NMOS device gates GC are capped with nitride 256 and nitride spacers 258, and the gaps between devices are planarized with BPSG oxide. The transistors are suitable adjusted to have the desired threshold voltage. There is no silicide used for GC and source drain regions. Nitride and oxide caps would prevent a silicide formation. There are no wells in the substrate. Lack of N-wells show there is only one type of FET possible with this construction (namely NFET).

Once the two wafers (or two separate die) are constructed, they are bonded together to obtain the required functionality. To bond, an adhesive handle wafer is attached from the top to the second pass gate wafer as shown in Fig-15. The P+ portion of the substrate is polished off leaving only the P- layer. To control NFET transistor properties, it is important to contact the substrate P- region. How this is achieved is not disclosed. Then a TEOS layer is deposited on the up-side-down P- exposed surface of the second wafer. This is then bonded to the first latch wafer using another bonding layer (col 9, line 26). In Fig-19, the P- substrate layer 312 is fully isolated by the TEOS regions 282, 314, OX, 294 below, and the oxide 328 and nitride cap layers 334 &

326 from above. Heat dissipation from switching circuits in this thermally isolated module is a problem. One with ordinary skill could not construct switching logic circuits in this pass gate layer due to lack of substrate potential control, lack of salicided GC poly, lack of salicided S/D regions, lack of N-wells to construct PFETs, and lack of substrate contact for thermal dissipation. Bertin does not construct logic circuits in this device, he only constructs pass gates.

After bonding, the substrate layers (288, 286 in Fig-15) of the first latch wafer are removed (col 9, line 45). One with ordinary skill would not be able to construct logic circuits on this latch layer either as the entire P-/P+ substrate is removed. Incomplete latch wiring is completed on the bottom exposed oxide layer (col 9, line 53). After the bottom wiring, the wafer is passivated at the bottom as shown in Fig-16. The pass gates bonded from the top are still not connected to the latches. The connection required is shown in Fig-2 wherein pass gates 140 and 138 have N+ junctions tied to vertical stack 134. This vertical construction is illustrated in Fig-17 & 18. The bonded wafer with bottom passivation is flipped to the pass gate layer on top, etching suitably selected holes 318 and filling those with metal 324. Fig-19 thru Fig-24 illustrates the numerous steps required to couple the latch wafer to the pass-gate wafer.

Finally, Bertin does not disclose how the decoding logic is constructed for the SRAM cell array. While it is important to have a very high density SRAM cell array, there has to be decoders that select columns and rows to reach an individual cell in the array. These nodes are denoted W/L, B/L and B/L bar in Fig-2 and Fig-25. Metal lines 394, 396 from top in Fig-25 contact drain nodes to form B/L and B/L bar, while long GC lines are used for W/L. There has to be sense amplifiers that detect the data state in each SRAM cell location. These circuits require logic, preferably CMOS logic circuits. CMOS logic requires N-wells and P-wells to construct PFET and NFET transistors respectively. N-well has to be biased to Vcc and P-well has to be biased to Vss voltage respectively to prevent latch-up. Bertin does not show how the P- body region 312 in Fig-17 is biased to ground. It is not shown how an N-well should be integrated to this very complex construction scheme. Furthermore, poly shown as GC in Fig-14 has to be doped with different dopant types for PFET and NFET devices. As GC is covered by nitride layer NIT 256 in Fig-14, it cannot be silicided to connect opposite doped poly in the same geometry.

All in all, Bertin constructs a very dense SRAM array by forming a latch wafer, a pass gate wafer, bonding the two together, and completing the local and global wiring required for the

SRAM array. There is no discussion on how to construct logic to decode the SRAM control signals.

In the independent claims 12, the applicant claims:

> 12. (Currently Amended) A method of forming a semiconductor latch for integrated circuits, said latch adapted to receive a first supply voltage and a second supply voltage substantially at a lower voltage level than said first supply voltage, the method comprising:
> depositing an isolation layer above a first module layer, said first module comprising a high mobility semiconductor substrate layer used to fabricate logic transistors; and
> depositing a semiconductor thin film layer; and
> fabricating a first and a second conducting path of a first inverter in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a first output, said second conducting path coupled between said second supply voltage and said first output; and
> fabricating a first and a second conducting path of a second inverter in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a second output, said second conducting path coupled between said second supply voltage and said second output.

First, applicant respectfully traverses the Section 102(b) and the alternative Section 103(a) rejections. For anticipation under 35 U.S.C. § 102(b), Bertin '169 patent must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present.

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
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> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
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> "The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required." In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicant also notes that the present rejection does not establish *prima facie* obviousness under 35 U.S.C. § 103 and M.P.E.P. §§ 2142-2143. The Examiner bears the initial burden to establish and support *prima facie* obviousness. *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976). To establish *prima facie* obviousness, three basic criteria must be met. M.P.E.P. § 2142.

First, the Examiner must show some suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to modify the reference so as to produce the claimed invention. M.P.E.P. § 2143.01; *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Second, the Examiner must establish that there is a reasonable expectation of success for the modification. M.P.E.P. § 2142.

Third, the Examiner must establish that the prior art references teach or suggest all the claim limitations. M.P.E.P. §2143.03; *In re Royka*, 180 U.S.P.Q. 580 (CCPA 1974).

The teachings, suggestions, and reasonable expectations of success must be found in the prior art, rather than in Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q.2d 1438 (CAFC 1991).

Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on all three of the above requirements.

A) Claim-12 102(b) rejection:

(i) Bertin does not demonstrate fabricating logic transistors. His construction comprises fabricating latch transistors (cross-coupled to form latches in a first chip), and pass gate transistors (NFET's to form the access transistor to latch) in a second chip. There is no explicit or implied reference on constructing the control logic transistors required for SRAM operation in his disclosure. One with ordinary skill would not be able to construct logic transistors either in the latch layer (lack of a substrate P-/P+ region), or in the pass gate layer (lack of N-well, silicide, P-well, substrate potential control, poor thermal dissipation, etc.).

(ii) Bertin does not demonstrate depositing a semiconductor thin film layer above (or below as the examiner noted) the module layer comprising pass gate transistors. Bertin bonds the second latch wafer below the first pass gate layer. This construction comprises a dual substrate silicon wafer construction, while the Applicant's method claim is with respect to a single substrate silicon wafer construction on which a second thin silicon layer is deposited.

(iii) Bertin does not demonstrate a thin film layer above or below for the inverter construction. The inverters are constructed on an epitaxially grown silicon layer. The height of the epi pillars are same as the nitride stripe thickness, stated as 0.4-1.0 um (col 5, line 62). The Applicant discloses film thicknesses in Eq-1 thru Eq-6, and the thicknesses in the discussion (page 27 and page 30) are in the range about 250 & 300 Angstroms (i.e. less than 0.05 microns). One with ordinary skill could not construct the epitaxy thickness to be 0.05 um in height as it

would have been impossible to get N+/P-/N+ or P+/N-/P+ doped layers and the required metal line contacts in the stack. Bertin at best has a thick epitaxy layer for latch inverter construction.

(iv) Bertin does not show SRAM latch inverters constructed above the logic transistors as the examiner has noted. Logic transistors switch during normal applications, and generate a high amount of heat. The power generated scales as $P \sim fCV^2$, where f is frequency, C is capacitance and V is voltage. This is the power consumed by the device at a given operating frequency that gets converted to heat. Silicon substrate is a good heat conductor. When the substrate is at the bottom, it is directly bonded to a heat sink plate and the generated heat is readily dissipated. If the logic circuits are constructed above an oxide insulating surface, the heat dissipation is blocked. There is a significant advantage in constructing SRAM cells above a logic layer that has the silicon substrate bonded to the heat sink of the package. One with ordinary skill would not be able to integrate Bertin SRAM cells with high speed logic circuits.

(v) With respect to Applicant's claim 14, Bertin is only able to use epitaxially grown silicon, and could not use a deposited silicon material of any nature.

(vi) With respect to Applicant's claim 15, Bertin does not demonstrate constructing latch conducting paths for NFET and PFET in a single geometry. The N+/P-/N+ FET is in a first geometry, and the P+/N-/P+ FET is in a second geometry. Each epitaxial pillar is grown in separate epitaxial steps in the process utilizing multiple pattering, etching and doping steps.

(vii) With respect to Applicant's claim 16, Bertin does not show a common gate for the inverter. In Bertin inverter, the drain of one inverter acts as the gate of the second inverter and the drain of the second inverter acts as the gate of the first inverter. This is illustrated in Fig-3B.

The Applicant respectfully submits that all of the independent claim 12 elements are not found in the Bertin '169 patent. Furthermore, the identical invention was not shown by Bertin as his patent pertains to bonding pass gates in a first wafer to latches in a second wafer to build high density SRAM cells, while the Applicant's invention pertains to constructing embedded SRAM cells above logic transistors. Withdrawal of the 102(b) objection on Applicant's claim 12, and those derived thereupon is respectfully requested.

B) Claim-12 103(a) rejection:

Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on all three requirements needed.

(i) There is no suggestion or motivation in Bertin '169 patent to modify the high density SRAM cell array to come up with the Applicant's vertically integrated thin film transistor SRAM cell array. In col 1, line 47, Bertin states:

> "Normally, the PFET is stacked above the NFET. Each such stacked pair forms a CMOS inverter. Two such stacked pairs are cross coupled as the cell latch. These cross coupled stacked transistor inverters form a very dense CMOS cell.
>
> However, the density realized from stacking the FETs may be offset by the resulting relatively poor electrical device characteristics of stacked devices (especially for the PFET) as compared to normal bulk FETs, which are typically twice as fast. Bulk FETs provide better performance than stacked device cells, but are larger, because of less efficient wiring."

In this passage, the normally stacked PFET is constructed in a thin film layer. The Applicant advocates constructing both NFET and PFET devices in the thin film layer, which is contrary to Bertin's teaching. Bertin teaches not to use thin film transistors period, even for the PFET. One with ordinary skill would be motivated away from the Applicant's disclosure.

(ii) There is no reasonable expectation of success for modifying Bertin to generate Applicant's claim. Bertin patent use extremely elaborated processing techniques to construct the latch wafer, bond the pass gate wafer to the latch wafer and provide local and global wiring. The Applicant does not advocate a two die bonding technique to construct thin film SRAM cells above logic transistors. Deposition and Bonding are entirely different techniques to construct stack geometries. Even if one could conceive how a pass gate layer can be simply deposited above the latch layer, or visa versa, the Applicant does not disclose a method to construct pass gates above latch inverters: the Applicant discloses a method to deposit pass gates and latch inverters in the same thin film layer, both located above a logic transistor layer. Bertin uses very elaborate glue technique to attach the two die, and a sequence of deposit, mask, etch techniques to connect the components in one die to the second. The Applicant's technique uses very few extra masking and processing steps and would cost only a small fraction of the cost involved with Bertin process.

(iii) The Bertin '169 patent does not teach or suggest all the claim limitations in Applicant's claim 12. This was discussed in detail under the earlier 102(b) rejection section. Specifically, Bertin does not have a thin film layer as discussed by the Applicant in his patent, nor does he use a deposition step to integrate the thin film layer. Bertin fails to show pass gates

and inverters constructed in the same thin film layer, both located above logic transistors used for high speed switching circuits.

In sum, the Office Action did not establish and support *prima facie* obviousness of claim 12 as required in *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976) because each of the three basic criteria was not met. Hence, claim 12 as well as those dependent thereupon are patentable over the references, and withdrawal of the objection is respectfully requested.

In the independent claims 20, the applicant claims:

> 20. (Currently Amended) A method of fabricating a semiconductor latch for an integrated circuit, comprised of:
> forming two inverters, said inverters cross-coupled to form a bi-stable latch; and
> supplying each of said inverters with a first supply voltage and a second supply voltage, said second supply voltage substantially lower than said first supply voltage level, and
> forming at least one of said inverters in a semiconductor thin film module, said module fabricated substantially above a semiconductor substrate module used to construct high performance switching logic circuits.

First, applicant respectfully traverses the Section 102(b) and the alternative Section 103(a) rejections.

1) Claim-20 102(b) rejection:

(i) Bertin does not demonstrate fabricating logic circuits. His construction comprises fabricating latch transistors (cross-coupled to form latches in a first chip), and pass gate transistors (NFET's to form the access transistor to latch) in a second chip. There is no explicit or implied reference on constructing the control logic transistors required for SRAM operation in his disclosure. One with ordinary skill would not be able to construct logic circuits either in the latch layer (lack of a substrate P-/P+ region), or in the pass gate layer (lack of N-well, silicide, P-well, substrate potential control, poor thermal dissipation, etc.).

(ii) Bertin does not demonstrate fabricating high performance switching logic circuits. High performance logic circuits require PFET and NFET fabrication with N-well and P-well regions. Both wells require very good potential control by appropriate contact and voltage bias techniques. Bertin does not show CMOS fabrication in the pass gate wafer, and has no substrate in the latch wafer to construct any circuit besides the inverter latches. High performance

switching circuits dissipate a high level of heat, and Bertin does not have an assembly in which the heat can dissipate. Both wafer die in Bertin is encapsulated with oxides and passivation, and there is no method of bonding the heat generating silicon substrate to a heat sink.

(iii) Bertin does not demonstrate fabricating an inverter in a thin film module. The inverters are constructed on an epitaxially grown silicon layer. The height of the epitaxial pillars is same as the nitride stripe thickness, stated as 0.4-1.0 um (col 5, line 62). The Applicant discloses film thicknesses in Eq-1 thru Eq-6, and the thicknesses in the discussion (page 27, line 10 and page 30, line 21) are in the range about 250 & 300 Angstroms (i.e. less than 0.05 microns). One with ordinary skill could not construct the epitaxy thickness to be 0.05 um in height as it would have been impossible to get N+/P-/N+ or P+/N-/P+ doped layers and the required metal line contacts in the stack. Bertin at best has a thick epitaxy layer for latch inverter construction, and does not have a thin film module.

(iv) Bertin does not show SRAM inverter module fabricated substantially above the substrate module as the examiner noted. The substrate polish techniques of both pass gate wafer and the latch wafer mandates the pass gate layer to be bonded above the latch layer. One could flip the die assembly upside down to have the latch wafer above the pass gate wafer. Then the logic layer as stated by the Applicant must reside in the latch wafer: but lack of a P-/P+ substrate prevent constructing logic in the latch layer. There is a significant advantage in constructing SRAM cells above a logic layer that has the silicon substrate bonded to the heat sink of the package. Power generated as heat from the switching logic transistors must be removed. Silicon substrate is a good heat conductor. When the substrate is at the bottom, it is directly tied to a heat sink and the generated heat is readily dissipated. If the logic circuits are constructed above an oxide insulating surface, the heat dissipation is blocked.

The Applicant respectfully submits that all of the independent claim 20 elements are not found in the Bertin '169 patent. Furthermore, the identical invention was not shown by Bertin as his patent pertains to bonding pass gates in a first wafer to latches in a second wafer for high density SRAM cells, while the Applicant's invention pertains to constructing embedded SRAM cells above logic transistors. Withdrawal of the 102(b) objection on Applicant's claim 20 is respectfully requested.

B) Claim-20 103(a) rejection:

Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on all three of the requirements needed.

(i) There is no suggestion or motivation in Bertin '169 patent to modify the high density SRAM cell array to come up with the Applicant's vertically integrated thin film transistor SRAM cell array, wherein at least one inverter is constructed above logic. In col 1, line 47, Bertin states:

> "Normally, the PFET is stacked above the NFET. Each such stacked pair forms a CMOS inverter. Two such stacked pairs are cross coupled as the cell latch. These cross coupled stacked transistor inverters form a very dense CMOS cell.
>
> However, the density realized from stacking the FETs may be offset by the resulting relatively poor electrical device characteristics of stacked devices (especially for the PFET) as compared to normal bulk FETs, which are typically twice as fast. Bulk FETs provide better performance than stacked device cells, but are larger, because of less efficient wiring."

In this passage, the normally stacked PFET is constructed in a thin film layer. The Applicant advocates constructing both NFET and PFET devices in the thin film layer, which is contrary to Bertin's teaching. Bertin teaches not to use thin film transistors even for the PFET. One with ordinary skill would be motivated away from the Applicant's disclosure.

(ii) There is no reasonable expectation of success for modifying Bertin to generate Applicant's claim. Bertin patent use extremely elaborated techniques to construct the latch wafer, bond the pass gate wafer to the latch wafer and provide local and global wiring. The Applicant does not advocate a two die bonding technique to construct thin film SRAM cells above logic transistors. Deposition and Bonding are entirely different techniques to construct stack geometries. Even if one could conceive how a pass gate layer can be simply deposited above the latch layer, or visa versa, the Applicant does not disclose a method to construct pass gates above latch inverters: the Applicant discloses a method to deposit pass gates and latch inverters in the same thin film layer, both located above a logic transistor layer. Bertin uses very elaborate glue technique to attach the two die, and a sequence of deposit, mask, etch techniques to connect the components in one die to the second. The Applicant's technique uses very few extra masking and processing steps and would cost only a small fraction of the cost involved with Bertin process.

(iii) The Bertin '169 patent does not teach or suggest all the claim limitations in Applicant's claim 12. This was discussed in detail under the earlier 102(b) rejection section. Specifically, Bertin does not have a thin film layer as discussed by the Applicant in his patent, nor does he use high performance switching logic circuits with SRAM cells. Bertin fails to show

pass gates and inverters constructed in the same thin film layer, both located above logic transistors used for high speed switching circuits.

In sum, the Office Action did not establish and support *prima facie* obviousness of claim 20 as required in *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976) because each of the three basic criteria was not met. Hence, claim 20 is patentable over the reference, and withdrawal of the objection is respectfully requested.

Allowable subject matter

The examiner noted that:

> 8. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the objection noted above.

The Applicant has herewith submitted reasons to request withdrawal to objections on independent Claim-12, which is the base claim for the dependent Claims 17-19. Withdrawal of this objection is respectfully requested on the condition of the requested withdrawal of the objections to Claim-12.

CONCLUSION

Applicant believes that the above discussion is fully responsive to all grounds of objections and rejections set forth in the Office Action.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the the Inventor Mr. Madurawe at (408) 737-8868.

Respectfully submitted,

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